A 6.5-mW Receiver Front-End for Bluetooth in 0.18-μm CMOS

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Abstract — **This paper describes the design of a low-IF receiver front-end for Bluetooth fabricated in a 0.18 μm CMOS technology. The chip includes an LNA and an image-reject mixer and provides a down-conversion gain to the 2 MHz IF of 21.4 dB, an image rejection of 28 dB and a NF of 13.9 dB consuming only 6.5 mW at 1.8 V.**

I. Introduction

Bluetooth is an industry standard for short-range wireless voice and data communication operating in the unlicensed 2.4 GHz ISM band [1]. It specifies a frequency-hopped, spread-spectrum system that support a raw data rate of 1 Mb/s. In order to enable low-power and highly integrated implementations, the radio specifications were deliberately made quite relaxed. Although some fully integrated CMOS transceivers were reported [2]-[5], they all consume more than 120 mW (in receive mode), a power consumption adequate for devices such as laptops, PDAs and mobile phones, but not quite adequate for other much smaller devices.

The design reported here is the result of a careful balance between power consumption and performance and targets applications such as wrist-watches and smart-cards, where power consumption and physical dimensions are of paramount importance. The presented chip includes what usually is the most power consuming part of the system, that is the receiver front-end.

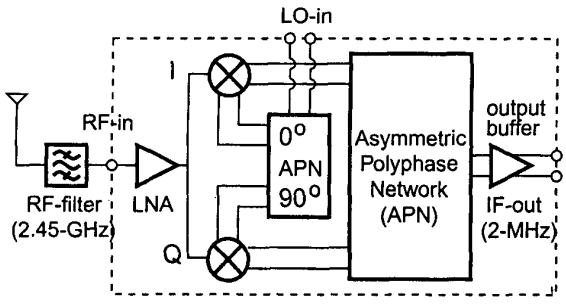

Fig. 1. Block diagram of the chip.

II. Architecture

Fig. 1 shows a functional block diagram of the receiver front-end. A low-IF architecture with an intermediate frequency of 2 MHz was preferred over the traditional superheterodyne as the physical dimensions of a passive high-Q channel-select filter such as [6] was judged unacceptable for the targeted applications. The direct-conversion architecture was also discarded mainly because of the prescribed GFSK modulation scheme. The spectrum of a GFSK modulated signal has in fact its maximum at the carrier frequency and requires therefore a complex DC-offset compensation scheme, whereas the required image rejection for a heterodyne solution is only 20 dB.

In order to fulfill type approval a Bluetooth receiver must provide a sensitivity of at least -70 dBm (0.1% BER), which translates in a NF of 26 dB and, on the other extreme of the dynamic range, it must provide an input-referred third-order intercept (iIP3) of -17.5 dBm (the NF and iIP3 values were calculated assuming a demodulator requiring 18 dB SNR). Although the relaxed noise requirements could be satisfied without the use of an LNA preceding the mixer, a preamplifier is anyway required to reduce the spurious LO signal emitted by the receiver. Any residual LO signal reaching the input of the front-end, being in the service band, would not be filtered out by the preselection filter and would therefore be radiated by the antenna.

III. Circuit Design

A. Preamplifier

The gain of the implemented preamplifier is 12 dB and was chosen so as to guarantee the system linearity requirements without the use of any gain-control system. Fig. 2 shows the topology of the amplifier. L_g and L_s together with the capacitance C_{gs} of transistor $M1$ form an impedance matching network used to produce the 50 Ω needed to properly terminate the preselection filter. L_d is used to tune-out the capacitance constituted by the input impedance of the following mixer in parallel with the drain-bulk parasitic capacitance of transistor $M2$. L_s is realized as a bondwire, whereas L_g and L_d are on-chip spiral inductors. Resistor R_d

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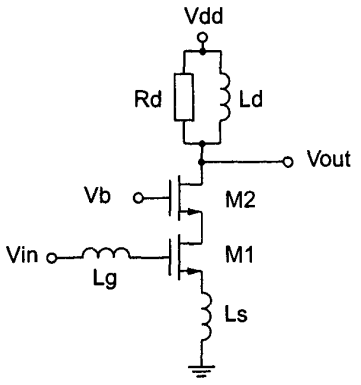

Fig. 2. Schematic diagram of the preamplifier.

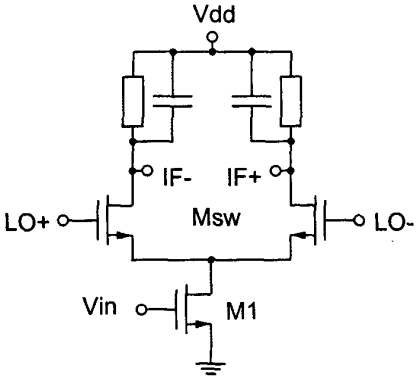

Fig. 3. Schematic diagram of the single-balanced mixer.

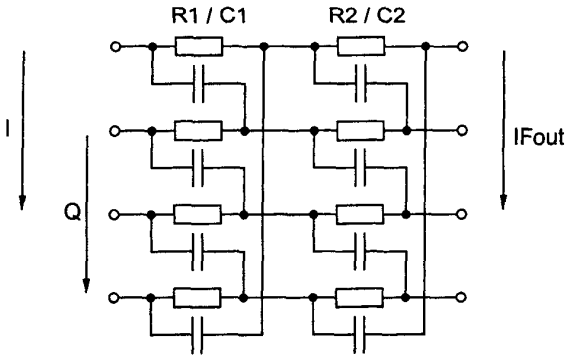

Fig. 4. Schematic diagram of the IF asymmetric polyphase filter.

is used to lower the Q of the load resonator and to precisely set the gain of the amplifier. Cascode transistor $M2$ is used to improve the unilaterality of the amplifier. The current required by the stage is 1.2 mA and is set by linearity requirements. Transistor $M1$ is in fact biased at the boundary between strong and moderate inversion ($V_{gs} - V_{th} \approx 80$ mV). A further reduction of the current (without a change in transistor geometry) would have made the linearity of the system dependent upon moderate inversion characteristics which are not well modeled and thus difficult to predict and to control. A simultaneous reduction of current and transistor width in such a way as to keep the transistor in strong inversion would have required impractical inductor values for the input matching network.

B. Image-Reject Mixer

The implemented image-reject mixer is constituted by two mixers (Fig. 3) and two asymmetric polyphase filters (Fig. 4). Single-balanced mixers are used as they require half the current of fully-balanced mixers for the same g_m. A disadvantage of the single-balanced structure with respect to the double-balanced one is the lack of isolation between the LO- and the IF-port. The strong LO signal present on the IF-path, if not properly suppressed, could saturate the active channel filter (not implemented) and desensitize the receiver. As the LO frequency is three decades higher than the IF, the LO signal is easily filtered out with a non-critical passive *RC* low-pass filter. In order to minimize coupling through the substrate the LO and the IF signals are differential. Each mixer consumes 1.2 mA and provides a voltage conversion gain of 10 dB.

One of the main noise contributors of the mixer, but also of the whole front-end is the $1/f$ noise of the switching transistors M_{sw}. This noise contribution could be lowered by increasing the width of the transistors. Using wider transistors would actually result in (i) a lower flicker noise current spectral density [7] and (ii) in a shorter time slot τ during which both transistors are conducting current. Both effects would contribute in reducing the noise generated by these transistors . It is in fact during the time slot τ that they are contributing most of their noise [8]. As the noise figure of the front-end is already 10 dB better than required, these transistors were kept rather narrow in order to provide a high LO-port impedance and thus spare current in the VCO or VCO-buffer driving the mixer.

To achieve the prescribed image-rejection of 20 dB we use two passive second order asymmetric polyphase filters [9]. One filter is responsible for the generation of the quadrature LO signals, whereas the other is used to combine the I and Q paths and suppress the unwanted sideband. The IF channel select filter has not been combined with the IF polyphase filter, as a complex domain channel filter requires twice as many OpAmps (and thus power) as a conventional filter [10]. Source followers with a gain of -2.1 dB buffer the IF signal in order to enable characterization of the front-end.

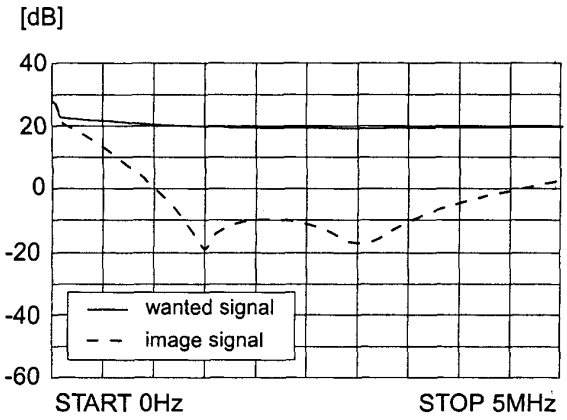

Fig. 5. Measured front-end conversion gain of wanted- and image-signal.

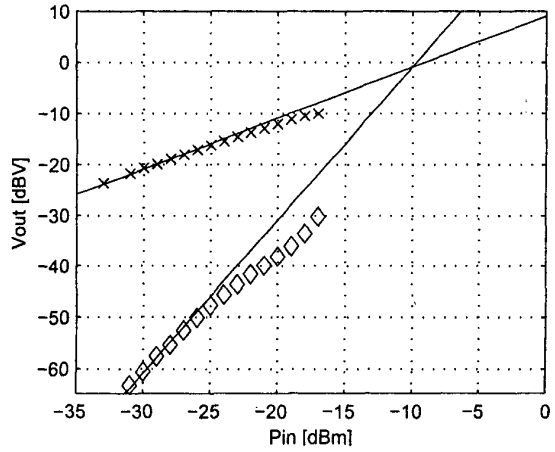

Fig. 6. IP3 based on measurements.

IV. Measurements

Measurements have been performed at the nominal 1.8 V supply on unpackaged chips bonded on a small PCB. Fig. 5 shows the measured conversion gain of both sidebands. The measurements have been performed with an external LO signal of 1 dBm at 2.445 GHz. The voltage conversion gain experienced by the upper sideband signal is 19.3 dB (including the output buffer). The image rejection at 2 MHz is 28 dB and is greater than 20 dB between 1 and 4.5 MHz. The LO-RF port isolation is 39 dB and the iIP3 and 1-dB iCP are -10 dBm and -18 dBm respectively (Fig. 6). The NF of the complete front-end is 13.9 dB and together with a preselection filter such as [6] results in a NF of 16 dB at the antenna. The current consumption of the front-end is 4.2 mA, 0.6 mA of which are consumed by the output test-buffer. The power consumption of the front-end core is thus 6.5 mW. A micrograph of the chip is shown in Fig. 7.

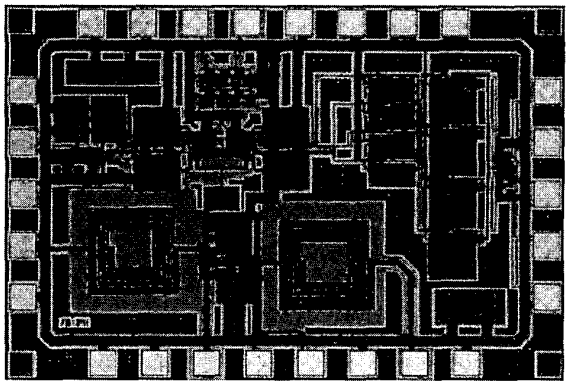

Fig. 7. Chip micrograph.

TABLE I.

Summary of Measured Performance (T=25°C).

Paramerer	Value	Unit
V_{dd}	1.8	V
I_{dd}	3.6	mA
Conversion-Gain	21.4	dB
Image-Rejection	28	dB
iIP3	-18	dBm
iCP	-10	dBm
NF	13.9	dB
LO-RF isolation	39	dB

V. Conclusion

A very low power low-IF front-end IC meeting Bluetooth specifications has been described. The circuit comprises a preamplifier and an image-reject mixer and is realized in a 0.18-μm CMOS technology. The targets of the design were: minimization of physical dimensions and minimization of power consumption. The first goal was achieved by the choice of a highly integrable architecture, whereas the latter was achieved by using simple circuits with commensurate characteristics and by using a deep-submicron technology. Table I. summarizes the performance of the 6.5 mW front-end.

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